Once an individual sub-module has passed the timing requirements and verifications, as determined in steps 66A-C, a gate-level netlist is provided in steps 68A-C to be integrated in step 70 with the other gate-level netlists of the other sub-modules to form a top-level design netlist. The integrated top-level design netlist is then tested in step 71 in the same manner as each of the individual sub-modules in steps 65A-C. It is determined in step 72 whether the integrated top-level netlist and design satisfies all of the top-level timing requirements and other verifications performed on the top-level final design. If it does not, the process returns to step 62 or steps 64A-C to re-perform the synthesis of the sub-modules.--

**IN THE CLAIMS:**

Please cancel claim 4 without prejudice or disclaimer.

Please amend claims 1, 5 and 7 as follows:

1. (Amended) A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining a plurality of sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system;

synthesizing gate-level designs of the sub-modules based on the determined time budgets for the individual sub-modules;

testing the gate-level designs for conformance with gate-level design requirements of the individual sub-modules, then integrating the gate-level designs of the individual sub-modules to form a top level design;

testing the top-level design for conformance with top-level design requirements; and

generating a top-level netlist when the top-level design conforms to the top-level design requirements.

5. (Amended) The method of claim 1, wherein testing the gate-level designs includes performing static timing analysis on the individual sub-modules for conformance with timing requirements for the individual sub-blocks.

7. (Amended) The method of claim 6, wherein the step of synthesizing is re-performed and the gate-level designs are retested in an iterative manner to verify conformance of the gate-level designs with the timing requirements of the individual sub-modules.

Please add new claims 10-17 as follows:

--10. A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining sub-module of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system

synthesizing gate-level designs of the sub-module based on the determined time budgets for the individual sub-modules;

integrating the gate-level designs of the individual sub-modules to form a top level design;

testing the top-level design for conformance with top-level design requirements;

generating gate-level netlists for the gate-level designs of each of the sub-modules; and

generating a top-level netlist when the top-level design conforms to the top-level design requirements.--

--11. The method of claim 10, wherein the step of integrating the gate-level designs includes integrating the gate-level netlists of the sub-modules.--